**(Tris) Jiayi Tian**

Email: 191180118@smail.nju.edu.cn | Mobile: 86-15542405069

**Education**

**Nanjing University Nanjing, China**

School of Electronic Science and Engineering Sept. 2019- Jul. 2023

* B.Eng., Major in VLSI Design & System Integration
* **Cumulative GPA: 4.51/5.0; Major GPA: 4.49/5.0 (Top 10% in the grade)**

**Research Experience**

**Low-bit Quantization Work of BERT in the NLP Area**

*Independent Project, Apr. 2021-Oct. 2022*

* Used Python and Pytorch to perform low-bit quantization in BERT models and enhance their efficiency and robustness.
* Investigate literature on Transformer-based models and learn about the model compression methods for BERT.
* Give reports biweekly on the project progress at the group meeting
* Proposed **Binary Ensemble BERT (BEBERT)**, a novel compression scheme to boost the efficiency and robustness of binary BERT. Our BEBERT outperforms the existing binary models by **2%~4%** in accuracy, reducing variance by around **60%**, and achieves **2x** acceleration in the training process.

**INT8 Quantization Work of BERT with Hardware Deployment**

*Member, Sept. 2021-Dec. 2022*

* Used Python and Pytorch to perform INT8 quantization in BERT models
* Used Matlab to achieve the BERT models' encoder layer for a better understanding of the attention mechanism
* Trying to use Verilog to deploy the BERT models' inference process on Hardware.
* Give team reports on the project progress in biweekly team meetings

**Optimization for phase solution in lensless system**

*Independent Project, Sept. 2022-March. 2023*

* Used Python and Pytorch to optimize phase solution in lensless system
* Trying to demonstrate objective functions for the backward propagation process.
* Give team reports on the project progress in biweekly team meetings

**VLSI Design Experiment**

*Individual assignment, March. 2022~June. 2022*

* Used Vivado and Cadence to devise efficient coding for computing 1-dimension convolution
* Proposed three optimization methods based on basic VLSI techniques, including pipeline, parallel, and transpose
* Wrote a report in 11 pages by Latex and got an A score

**Verilog Design Experiment**

*Member, Mar. 2021-Jun. 2021*

* Used Quartus and Intel Cyclone5 Series' FPGA to complete a VGA display clock on the monitor, which can set time via keyboard
* Responsible for accomplishing the VGA display, mainly used RAM and sequential logic analysis for designing
* Wrote a report in 17 pages by Latex and got an A+ score

**Publications**

* **Jiayi Tian**, Chao Fang, Haonan Wang and Zhongfeng Wang. "BEBERT: Efficient and robust binary ensemble BERT." *IEEE Conference on Acoustics, Speech, and Signal Processing (ICASSP). 2023* [submitted]

**Technical Skills**

* Programming and HDL:

Advanced in C/Matlab, Proficient in Verilog, Python/Pytorch, Familiar with C++

* Hardware design and simulation skills:

Advanced in Vivado/Quartus/Modelsim, Altium Designer, and Multisim, Familiar with SPICE

* TOEFL 102; GRE 153+170

**Honors and Awards**

* National Undergraduate Electronic Design Contest, The 2nd Prize in Jiangsu Province, Nov. 2021(30%)
* National Undergraduate Electronic Design Contest, The 2nd Prize in Jiangsu Province, Oct. 2020(30%)
* People's Scholarship, The 2nd Prize in NJU, Nov. 2020(10%)
* Jinxiao Company Scholarship, Nov. 2021(5%)
* People's Scholarship, The Academic Competition Award, Nov. 2021(5%)
* Excellent Organization Award, Student Union in Sch of Elec Sci and Eng., NJU, Sept. 2020 (20%)
* Excellent Department Director, Student Union in Sch of Elec Sci and Eng., NJU, Oct. 2020 (15%)
* Excellent Volunteer Prize, NJU, Dec. 2021 (<1%)
* Excellent Volunteer Prize on the school's 120th anniversary, Sept. 2022 (<1%)